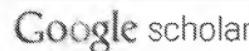


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 ... load/ store using their last effective address and a ... Predicted loads and stores are issued speculatively ... Instructions that depend on speculative loads are also ...

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... the thread context with the address of the ... Speculative threads must not update the architectural state, for example, by executing a store instruction. ...

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 ... commit speculative state, and exit speculative critical section ... is elided speculatively, and future store matching the ... load (ldl_l) to an address is followed ...

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 ... When a new thread is spawned, the effective address of each store instruction is predicted as the ... type of trace, the control flow of speculative loop traces ...

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... potentially increase the overlap available to stores and address the store latency responsible ... PC and SC, the two techniques of speculative retirement and ...

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... To initialize a **speculative** promotion, a spe- cial map ... the data at the given memory
address resides in ... are essentially just special load and **store** operations. ...
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... An interlock through memory occurs whenever an earlier **store instruction** with a ... If
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... for a superscalar processor sup- porting **speculative** execution. ... buffer for the return
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